Exhibit 3

DFI

DDR PHY Interface

DFI 4.0 Specification

APRIL 27, 2018

2.0 Architecture

The DFI specification requires a DFI clock and DFI-defined signals that must be driven directly by registers referenced to a rising edge of the DFI clock. There are no rules dictating the source of the DFI clock, nor are there restrictions on how the DFI-defined signals are received. For DFI interoperability between the MC and the PHY, ensure compatibility in:

- Signal widths
- Interconnect timing
- Timing parameters
- Frequency ratio
- Function

Interconnect timing compatibility between the MC and the PHY at target frequencies is determined by the specification of the output timing for signals driven and the setup and hold requirements to receive these signals on the DFI per device, as defined by the device.

The DFI specification does not dictate absolute latencies or a fixed range of values that must be supported by each device. Certain DFI timing parameters can be specified as fixed values, maximum values, or as constants based on other values in the system.

DFI timing parameters must be held constant while commands are being executed on the DFI bus; however, if necessary, DFI timing parameters may be changed during a frequency change or while the bus is in the idle state. For more information on timing, refer to Section 5.0, “Signal Timing”.

The DFI specification identifies the DFI signals relevant to a specific implementation based upon support for specific DRAM device(s), optional features and frequency ratio. For more information on which signals are relevant to a specific implementation, refer to Table 3, “DFI Signal Requirements”.

The MC and the PHY must operate at a common frequency ratio. For matched frequency systems, the DFI write data bus width is generally twice the width of the DRAM data bus. For frequency ratio systems, the DFI write data bus width will be multiplied proportional to the frequency ratio to allow the MC to send all of the DRAM-required write data to the PHY in a single DFI clock cycle. The write data must be delivered with the DFI data words aligned in ascending order.

- In a matched frequency system, the MC and the PHY operate with a 1:1 ratio.
- In a frequency ratio system, the MC and the PHY operate with a common frequency ratio of 1:2 or 1:4; the PHY must be able to accept a command on any and all phases. The frequency ratio depends on the relationship of the reference clocks for the MC and the PHY.
- Phase-specific signals with a suffix of “_pN”, with the phase number N (e.g., **dfi_wrdata_pN**), replace the matched frequency signals for the control, write data, read data and status interface signals. Phase-specific signals allow the MC to drive multiple commands in a single clock cycle.
- Data word-specific signals with a suffix of “_wN”, with the DFI data word number N (e.g., **dfi_rddata_wN**), replace the matched frequency signals for the read interface to distinguish how DRAM words are transferred across the DFI bus.
- Variable pulse width-specific signals with a suffix of “aN”, with the PHY clock cycle N (e.g., **dfi_alert_n_aN**), replace the matched frequency signals for the status interface to maintain the pulse width during transmission of error signals from the memory system to the PHY.

For all signal types, the suffix for phase 0/data word 0/clock cycle 0 is optional.

For more information on frequency ratios, refer to Section 4.9, “Frequency Ratios Across the DFI”.

2.1 Optional Protocols

Optional protocols handle data bus inversion (DBI), cyclic redundancy check (CRC), system frequency change, command/address (CA) parity, low power and the error interface. For more information on optional protocols, refer to Section 4.4, “Data Bus Inversion”, Section 4.5.3, “Cyclic Redundancy Check”, Section 4.10, “Frequency Change”, Section 4.11, “CA Parity Signaling and CA Parity, CRC Errors”, Section 4.12.3, “Initiating a Training Operation” and Section 4.14, “Error Signaling”.

2.2 DFI Feature Requirements

The DFI specification defines the MC-PHY interface for numerous memory protocols and topologies. Not all DFI features are applicable or required for any particular memory sub-system. Features are divided into global and memory-specific features to aid interoperability and optimal system design.

2.2.1 Global Features

Global features apply to all memory topologies. While these features are valid across all memory sub-systems, they are not always required. For example, any system can utilize “low power control” to reduce system power. However, the requirement of “low power control” is based on system trade-offs and constraints that are outside the scope of DFI. The list of global features are:

- Frequency ratios across DFI
- Frequency change
- Low power control
- Error signaling
- Update interface
- PHY master interface
- Clock disabling
- Data bit enable
- DFI disconnect
- Independent channel support

For specific signal requirements, refer to Table 3, “DFI Signal Requirements”.

2.2.2 Memory Topology-Specific Features

A subset of DFI features is not globally applicable to all memory sub-systems. A matrix of memory topology and features is defined in Table 2, “Features by Memory Topology”. While the feature matrix defines when a feature applies to a specific memory topology, each feature is not necessarily required. Specific feature requirements are based on system trade-offs and constraints that are outside the scope of DFI. For specific signal requirements per feature, refer to Table 2, “Features by Memory Topology”.

TABLE 3. *DFI Signal Requirements*

dfi_ras_n_*pN*	**t_{ctrl_delay}**	Required for DDR1, DDR2, DDR3, DDR4 and LPDDR1 DRAMs. [b] Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]	Required for DDR1, DDR2, DDR3, DDR4 and LPDDR1 DRAMs. [b] Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]
dfi_reset_n_*pN*	**t_{ctrl_delay}**	Required for DDR3, DDR4 and LPDDR4 DRAMs. [b] Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]	Required for DDR3, DDR4 and LPDDR4 DRAMs. [b] Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]
dfi_we_n_*pN*	**t_{ctrl_delay}**	Required for DDR1, DDR2, DDR3, DDR4 and LPDDR1 DRAMs. [b] Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]	Required for DDR1, DDR2, DDR3, DDR4 and LPDDR1 DRAMs. [b] Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]
Write Interface Group			
Signal	**Associated Parameters**	**MC**	**PHY**
dfi_wrdata_*pN*	**phy_{crc_mode}** **t_{phy_wrdata}** **t_{phy_wrlat}**	Required for all DRAMs. Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]	Required for all DRAMs. Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]
dfi_wrdata_cs_*pN*	**$t_{phy\_wrcsgap}$** **$t_{phy\_wrcslat}$**	Required for all DRAMs if any of the training features are supported, otherwise, optional. Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]	Optional. Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]
dfi_wrdata_en_*pN*	**dfi_{rw_length}** **phy_{crc_mode}** **t_{cmd_lat}** **$t_{phy\_crcmax\_lat}$** **$t_{phy\_crcmin\_lat}$** **t_{phy_wrdata}** **t_{phy_wrlat}** **t_{wrdata_delay}**	Required for all DRAMs. Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]	Required for all DRAMs. Suffix (_pN) required for frequency ratio systems to replicate information across the phases. [a]

However, in some cases, the devices may define the parameter differently such that the devices can still operate together but the differences would be resolved at the bus interconnection of the devices. For example, in an ECC system, the two devices might place the ECC data in different locations within the data bus, which can be resolved by interconnecting the devices to the bus for aligning these signals as necessary.

The programmable parameters associated with the status interface are listed in Table 17, “Status Interface Programmable Parameter”.

TABLE 17. *Status Interface Programmable Parameter*

Parameter	Defined By	Description
dfi$_{\textbf{data\_bit\_enable}}$	MC/PHY	Defines the bits that are used for transferring valid data on both the **dfi_wrdata** and **dfi_rddata** buses. This parameter is defined by both the MC and the PHY. The parameter can have different values for different operating modes for each device. The parameter width is defined as the DFI data width.
phy$_{\textbf{freq\_range}}$	PHY	Defines the range of frequency values supported by the PHY. The frequency range must be a number between 1 and 32 inclusive and must start from the value of ZERO to the defined range. The PHY may only support a subset of these frequencies and the PHY must clearly define supported encodings.

3.6 DFI Training Interface

The DFI training interface enables increased accuracy at higher speeds in the alignment of critical timing signals on DDR3, DDR4, LPDDR2, LPDDR3 and LPDDR4 DRAMs; the interface includes signals, timing parameters and programmable parameters.

The DRAM type and system configuration determine the types of training available to a system; a system may or may not utilize each type of training. If training is supported, the system may utilize DFI training or support a different training method. There are four training operations; the first two operations (gate training and read data eye training) are collectively referred to as “read training”.

1. Gate training, used by DDR3, DDR4, LPDDR2, LPDDR3 and LPDDR4 DRAMs.
2. Read data eye training, used by DDR3, DDR4, LPDDR2, LPDDR3 and LPDDR4 DRAMs.
3. Write leveling, used by DDR3, DDR4, LPDDR3 and LPDDR4 DRAMs.
4. CA training, only applicable to the MCs and PHYs that support LPDDR3 and LPDDR4 DRAMs.

Support for each training operation is enabled or disabled through the corresponding programmable parameter and the enable may be implemented as programmable registers within the device.

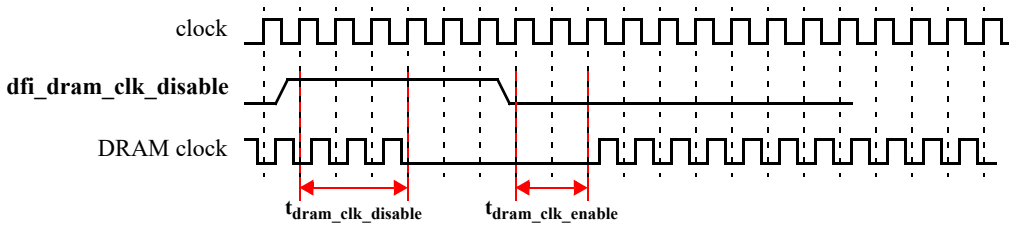
The read training, write leveling and CA training signals that communicate from the MC to the PHY are multiply driven inside the MC to allow a direct connection from the MC to each PHY data slice and the signals must be driven with the same value.

The read training, write leveling and CA training signals that communicate from the PHY to the MC may be individually driven by each PHY data slice or collectively driven as a single signal.

More information on the training interface is provided in Section 4.12.1, “Training Operations in DFI Training Mode”. The signals, timing parameters and programmable parameters for the training interface are listed in Table 18, “Training Interface Signals”. The timing parameters associated with the training interface are listed in Table 19, “Training Interface

the **dfi_dram_clk_disable** signal affects the DRAM clock and $\mathbf{t_{dram\_clk\_enable}}$ sets the number of cycles required for the DRAM clock to be active again.

FIGURE 37. *DRAM Clock Disable Behavior*



4.9 Frequency Ratios Across the DFI

In a DDR memory subsystem, it may be advantageous to operate the PHY at a higher frequency than the MC. If the PHY operates at a multiple of the MC frequency, the PHY transfers data at a higher data rate relative to the DFI clock and the MC has the option to execute multiple commands in a single DFI clock cycle. The DFI is defined at the MC to PHY boundary and therefore operates in the clock frequency domain of the MC.

The MC clock is always the DFI clock and all DFI signals are referenced from the MC clock.

The DFI specification supports a 1:1, 1:2 or 1:4 MC to PHY frequency ratio, defining the relationship of the reference clocks for the MC and the PHY. The DFI DDR PHY clock is always the same frequency as the DRAM clock, which is 1/2 the data rate for the memory.

DFI signals may be sent or received on the DFI PHY clock, provided the signals reference the rising edge of the DFI clock and the clock is phase aligned. The MC communicates frequency ratio settings to the PHY on the **dfi_freq_ratio** signal. This signal is only required for devices using this frequency ratio protocol.

The frequency ratio protocol affects the write data and read data interfaces, including read data rotation and resynchronization. Frequency ratio also affects CA and CRC parity errors.

For information on how frequency ratio affects CA and CRC parity errors, refer to Section 4.11.3, “CA Parity and CRC Errors in Frequency Ratio Systems”.

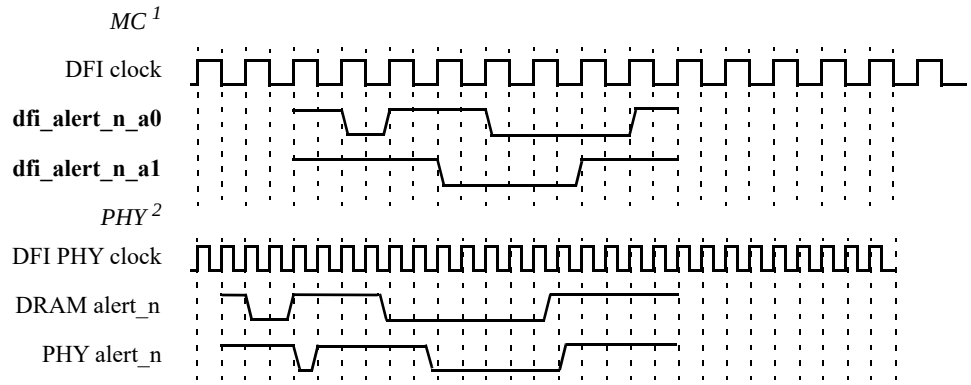
4.9.1 Frequency Ratio Clock Definition

The DFI clock and the DFI PHY clock must be phase-aligned and at a 1:2 or 1:4 frequency ratio relative to one another. Some DFI signals from the MC to the PHY must communicate information about the signal in reference to the DFI PHY clock to maintain the correct timing information. Therefore, the DFI PHY clock is described in terms of phases, where the number of clock phases for a system is the ratio of the DFI PHY clock to the DFI clock.

Figure 38, “Frequency Ratio 1:2 Phase Definition” and Figure 39, “Frequency Ratio 1:4 Phase Definition” show the clock phase definitions for 1:2 and 1:4 frequency ratio systems.

relate to the phase of assertion on the DRAM bus and therefore the assertion of **dfi_alert_n_a0** is not directly related to the phase of the write data.

FIGURE 59. ***dfi_alert_n_aN** with 1:2 Frequency Ratio*



NOTE: This timing diagram includes both the MC timing and an illustration of how the PHY interprets the MC timing in the PHY clock domain.

1. In the MC clock diagram, the timing shows the DFI bus signaling.
2. In the PHY clock diagram, the timing illustrates how the PHY interprets the DFI bus. PHY timing is shown for illustrative purposes only.

4.12 DFI Training Operations

DFI read and write training operations can increase accuracy of signal placement at higher speeds in DDR3, DDR4, LPDDR2, LPDDR3 and LPDDR4 systems. CA training optimizes the CA bus setup and hold times relative to the memory clock.

The DFI has five training operations to support CA training, read training, write DQ training, write leveling. “Read training” collectively refers to two operations - gate training and read data eye training. “CA training” refers to CA data eye training for LPDDR3 memories and to both CA data eye and VREF value training for LPDDR4 memories. For more information on the training operations and to identify operations that correspond to specific devices, refer to Section 3.6, “DFI Training Interface”.

For DFI compliance, the MC and the PHY may support either “ PHY Independent Mode” = or “DFI Training Mode” for the applicable training operations and the mode is set per operation.

Support for the defined state of each programmable parameter must be defined by each device and may be implemented as programmable registers within the device. The parameter is defined as a single enable bit indicating whether or not the corresponding DFI training operation (CA training, gate training, read data eye training, write DQ training or write leveling) is enabled.

4.12.1 Training Operations in DFI Training Mode

In DFI training mode, the MC sets up the DRAM for the training operation and periodically issues read commands, write bursts, write strobes or calibration commands as applicable. The PHY is responsible for determining the correct delay programming for each operation. The PHY evaluates the data returned from the commands, adjusts the delays and evaluates the results to locate the appropriate edges. The MC assists by enabling and disabling the leveling logic in the DRAMs and the PHY and by generating the necessary read commands, mode register reads, write bursts or write strobes.

The PHY informs the MC when it has completed training, which triggers the MC to stop generating commands and to return to normal operation.

The MC must complete all transactions in progress to memory prior to initiating any of the training operations. Once any of the enable signals are asserted, the PHY should immediately enable the associated logic. During training, the MC does not use the memory response from the PHY. Therefore the only relevant DFI timing parameters are:

- CA training: $\mathbf{t_{calvl\_cc}}$ (minimum delay between calibration commands)
- Read training: $\mathbf{t_{rdlvl\_rr}}$ (minimum delay that the MC should wait between issuing reads for DDR3 and DDR4 memory systems or mode register reads for LPDDR2, LPDDR3 and LPDDR4 memory systems)
- Write DQ training: $\mathbf{t_{wdqlvl\_rw}}$ (minimum delay from the last read in a calibration sequence to the first write in the next calibration sequence) and $\mathbf{t_{wdqlvl\_ww}}$ (minimum delay between write commands)
- Write leveling: $\mathbf{t_{wrlvl\_ww}}$ (minimum delay between write strobes)

The MC continues to drive subsequent CA training calibration commands every $\mathbf{t_{calvl\_cc}}$ cycles, subsequent read leveling commands every $\mathbf{t_{rdlvl\_rr}}$ cycles, subsequent write DQS training/leveling commands every $\mathbf{t_{wdqlvl\_ww}}$ cycles, or subsequent write level strobes every $\mathbf{t_{wrlvl\_ww}}$ until the PHY drives all bits of the response signal high.

Multiple training sequences can be defined, with the sequence information supplied by either the MC or the PHY. The MC must provide flexibility to run training sequences required by the PHY and should not dictate a set of sequences. The PHY determines the sequences necessary to accomplish training. Both the MC and the PHY need to be aware of the defined training sequences and the specific sequence required for each training operation.

Whether the MC or the PHY initiates the training sequence, the MC asserts the enable signal to initiate or accept the training sequence, and the MC holds the enable signal asserted until the current training operation completes. The DFI training requires the MC to support the training sequences to the PHY by generating MRW commands, toggling the enable parameter, generating the appropriate strobe signals and evaluating the response. The PHY is responsible for adjusting the DLL delays and evaluating the responses from memory. When the PHY is satisfied with the training sequence, a completion response is sent back to the MC.

For DDR4, training sequence accuracy is increased with a selection of encodings. The MC determines a sequence of up to four unique, non-default Multi-Purpose Register (MPR) values and formats and drives the **dfi_lvl_pattern** signal to communicate the sequence to the PHY to indicate the training pattern that is currently active.

4.12.2 Training Operations in PHY Independent Mode

In PHY Independent mode, the PHY supports training independent of the DFI signaling. In this case, the associated training interface is not used, and the MC should be capable of generating the required MRS commands to enter or exit the test modes of the DRAMs without the training interface signals.

4.12.3 Initiating a Training Operation

The MC or the PHY may initiate any training operation, depending on which training modes are supported. Training may be executed during initialization, frequency change or during normal operation. In DFI training mode, the MC is responsible for initiating gate training, read data eye training and/or write leveling required during initialization or frequency change. The PHY should not request training or leveling during initialization; if the PHY requests training during a frequency change, the PHY must assert it prior to asserting **dfi_init_complete**. In PHY independent mode, the PHY is responsible for all training/leveling as applicable.

The MC can initiate read training by driving the relevant bit (or bits) of the **dfi_rdlvl_en** signal, which is used for enabling the read training logic in the PHY independently for each slice, as Figure 60, “Read Data Eye Training Request Timing” illustrates. The PHY can also initiate read training on a slice by driving the appropriate bit of the **dfi_rdlvl_gate_req** or **dfi_rdlvl_req**. The MC will need to respond to this read training request signal assertion by asserting appropriate bit (or bits) of the **dfi_rdlvl_en** signal. If multiple slices must be enabled together, the user can specify the grouping in the $\mathbf{mc}_{\mathbf{rdlvl\_slice\_group[n]}}$ and/or $\mathbf{phy}_{\mathbf{rdlvl\_slice\_group[n]}}$ parameter.

During read training, the **dfi_rddata_valid** and **dfi_rddata** signals are ignored. All evaluations and delay changes are handled within the PHY. When the PHY finds the necessary edges and completes the read training, the PHY should drive the corresponding **dfi_rdlvl_resp** signal to ’b01, which informs the MC that the procedure is complete for that slice. The MC should then de-assert the set bit (or bits) of the **dfi_rdlvl_en** signal. When the **dfi_rdlvl_en** signal bit (or bits) de-asserts (de-assert), the PHY should stop driving the **dfi_rdlvl_resp** signal.

4.12.4.1 Gate Training

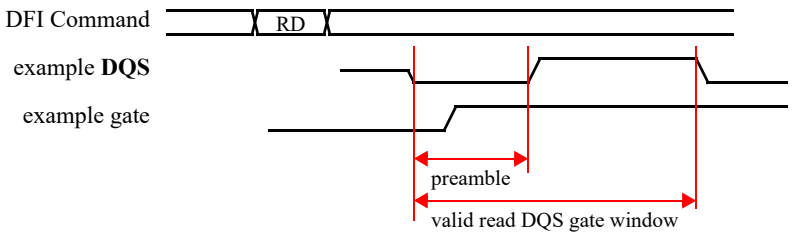
The goal of gate training is to locate the setting at which the initial read DQS rising edge aligns with the rising edge of the read DQS gate. Once this setting is identified, the read DQS gate can be adjusted to the approximate midpoint of the read DQS preamble prior to the DQS.

To indicate proper alignment of the gate to the first read DQS, the gate training operation requires that the read DQS gate be placed within the bounds of the beginning of the read DQS preamble and the falling edge of the first read DQS. Placing the gate within the bounds of the timing window may require another alignment method or may require running gate training iteratively.

The gate training signals are: **dfi_rddata_en**, **dfi_rdlvl_gate_en**, **dfi_rdlvl_gate_req**, **dfi_rdlvl_resp** and the DFI command bus. The corresponding mode parameter is $\mathbf{phy}_{\mathbf{rdlvl\_gate\_en}}$. When the PHY initiates gate training, the PHY can optionally send the **dfi_phy_rdlvl_gate_cs** signal to indicate the targeted chip select. The MC transfers the **dfi_rddata_cs** signal to identify the chip select currently being trained.

Figure 61, “Gate Leading DQS Timing” is an example of gate training.

FIGURE 61. *Gate Leading DQS Timing*



4.12.4.2 Data Eye Training

The goal of data eye training is to identify the delay at which the read DQS rising edge aligns with the beginning and end transitions of the associated DQ data eye. By identifying these delays, the system can calculate the midpoint between the delays and accurately center the read DQS within the DQ data eye.

The read data eye training signals are: **dfi_rddata_en**, **dfi_rdlvl_en**, **dfi_rdlvl_req**, **dfi_rdlvl_resp**, **dfi_lvl_pattern** and the DFI command bus. The corresponding mode parameter is $\mathbf{phy}_{\mathbf{rdlvl\_en}}$. When the PHY initiates data eye training, the

TABLE 44. *Data Calibration Pattern*

Pattern	Bit Time 0	Bit Time 1	Bit Time 2	Bit Time 3
"A" (MR32)	**1**	**0**	**1**	**0**
"B" (MR40)	**0**	**0**	**1**	**1**

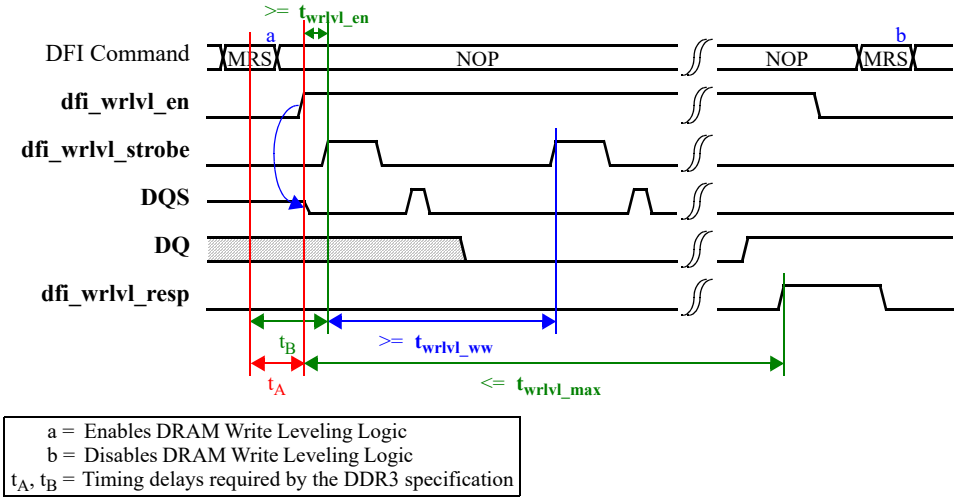
4.12.5 Write Leveling

The goal of write leveling is to locate the delay at which the write DQS rising edge aligns with the rising edge of the memory clock. By identifying this delay, the system can accurately align the write DQS within the memory clock.

The signals used in write leveling are: **dfi_wrlvl_en**, **dfi_wrlvl_req** and **dfi_wrlvl_strobe**. The corresponding parameter is $\mathbf{t_{wrlvl\_en}}$. When the PHY initiates write leveling, the PHY can optionally send the **dfi_phy_wrlvl_cs** signal to indicate the targeted chip select. For more information on write leveling signals, refer to Section 3.2, "Write Data Interface" and for more information on the **dfi_phy_wrlvl_cs** signal, refer to Table 18, "Training Interface Signals".

Figure 69, "Write Leveling in DFI Training Mode" demonstrates write leveling in DFI training mode. The MRS commands are used to enable and disable the write leveling logic in the DRAMs and the **dfi_wrlvl_en** signal is used for enabling or disabling the write leveling logic in the PHY.

FIGURE 69. *Write Leveling in DFI Training Mode*



LPDDR4 requires two DQS pulses. To allow two or more DQS pulses to be driven to the DRAM, during DFI write leveling, **dfi_wrlvl_strobe** can be driven for multiple clocks. For DFI4.0, each cycle that the **dfi_wrlvl_strobe** signal is driven generates a single DQS pulse. To support frequency ratio, the **dfi_wrlvl_strobe** signal is a phased signal. Figure 70, "DFI Write Leveling Interface with LPDDR4 Support" demonstrates write leveling in DFI training mode with LPDDR4 support.